Boundary scan based test system for TRIAX
using VarioTAP

The case:
DSE Test Solutions (DSE) has collaborated with TRIAX for many years as supplier of test solutions to TRIAX production test.
When TRIAX developed their new digital headend pro ducts for SMATV reception and distribution system, it was clear the limitations when using traditional boundary scan would make the test time too long and not give the required test coverage. A solution using VarioTAP in combination with boundary scan was selected.
The TRIAX system is based on a backend module for their headend system with an ARM.9 processor for module control and a FPGA for signal processing and 4 MPEG decoders.

Bent Rytter, R&D Project Manager at TRIAX says:
"We have worked with DSE for many years and see DSE as a competent and flexible partner to work with who always offer good service"

The advantage of the VarioTAP technology:
VarioTAP is a revolutionary technology for the fusion of Boundary Scan and processor emulation. It uses VarioTAP models to adapt platform modules to the target processor. The models are modularly defined as intelligent software IP and basically offer a multi-level functional structure.

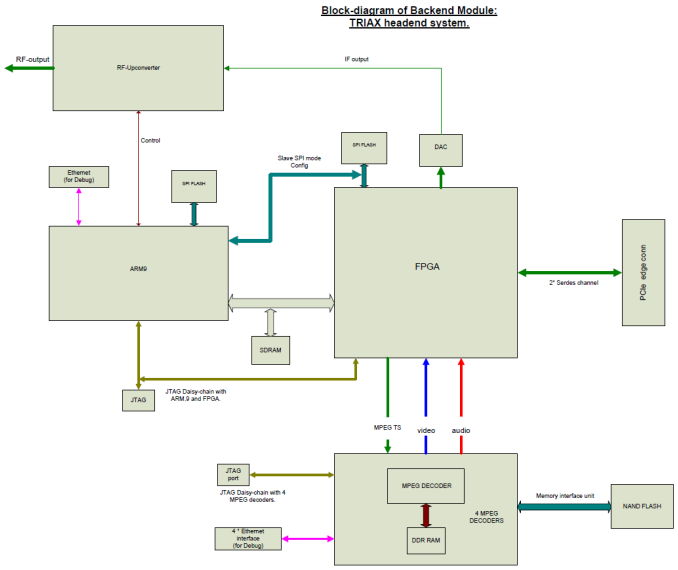
- core-assisted flash programming / PLD programming
- bus emulation test / system emulation test
- Embedded Diagnostics Test (EDT)

DSE is a GATE partner with Göpel Electronic and in cooperation with EP-TeQ and Testonica the necessary VarioTAP models was developed and implemented by DSE.

The project included development of a backend module for TRIAX headend system that has an ARM.9 processor for module control, FPGA for signal processing and 4 MPEG decoders. There are 2 JTAG ports on the board.

The ARM.9 was connected with the FPGA on the first daisy-chain. We do a traditional BSCAN infrastructure and interconnection test of the 2 devices and then load the VarioTAP model when we want to program the SPI devices for the ARM.9 and the FPGA.

Previously we have done the programming of the SPI devices with traditional BSCAN and have in a given example used up to 15 minutes to program 1,6Mbytes to single SPI device (JTAG_TCK = 15MHz),
but have reduced this programming time to under 5 minutes for programming of around 8Mbytes (JTAG_TCK = 35MHz) to the 2 devices in our present



application by using a VarioTAP model on the ARM.9. The second daisy-chain connects 4 MPEG decoders on the same daisy chain. This part of the board was very challenging since we could not use traditional BSCAN to test the board. The producer of the MPEG decoder was, due to some technical issues with the chip, not able to provide a traditional working solution for using the BSCAN mechanism of the chip (e.g. no .bsdl file, etc). We decided to ask Göpel and hence Testonica if they were able to make VarioTAP models of the MPEG decoder and they took up the challenge to design the models that will be used to test the 4 MPEG decoders and interfaces to their DDR RAM. Programming of the NAND flash which the 4 devices share, is done via the MIU of the first MPEG decoder using a script provided by the chip vendor. The script first loads images (around 13Mbytes) to DDR and uses one of these images to program the NAND flash afterwards (does BAD block and ECC checks).

For more information about VarioTAP technology see www.goepel.com

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